Abstract of the Disclosure

Disclosed are a multi-chip package and a method for manufacturing the multi-chip package. The multi-chip package comprises: a circuit substrate consisting of first, second and third areas which surround three sides of the multi-chip package; and at least two semiconductor chips which are positioned within an internal space of the package defined by the internal surfaces of the above three areas, wherein the semiconductor chips are physically bonded and electrically connected to each other. The method for manufacturing a multi-chip package comprises the steps of: providing a circuit substrate matrix formed with a plurality of unit circuit substrates, each substrate consisting of first, second and third areas; bonding semiconductor chips each unit circuit substrate, so that those chips are physically bonded and electrically connected to the unit circuit substrate; separating unit circuit substrates from the circuit substrate matrix; and folding the unit circuit substrate.